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A High-Resolution Supply Voltage Sensor Design and Its Performance Evaluation on an FPGA

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Abstract

Nowadays, integrated circuits (ICs) have higher integration densities. The simultaneous switching activities that are synchronized with a single global clock is one of the main causes that produce voltage drops across the power distribution network (PDN) of the ICs. Since the drop increase the delay of circuits, such drops may cause the timing failures that lead to the malfunctions of an IC. Therefore, a tool that supports for debugging the failures is essential. This paper presents a high-resolution supply voltage sensor that can be applicable for debugging timing failures at real-time, or determining the timing margins for the timing critical designs. Our supply voltage sensor is made up by using standard Look-up Table (LUT) cells, and dedicated carry cells with high-speed propagation delays. The experiments show that the voltage resolution of our supply voltage sensor is about 3.3mV on a Xilinx FPGA Spartan-6 (XC6SLX9).

요 약

고집적의 집적회로 상에서 클록에 의해 동기화되어 동시에 발생하는 스위칭은 집적회로의 전력분산망(PDN, Power Distribution Network)에 전압강하를 유도할 수 있으며, 이러한 전압강하는 회로지연에 영향을 주어 회로의 기능적 장애를 유발할 수 있다. 본 논문에서는 회로의 타이밍에 영향을 주는 전압강하를 실시간으로 평가할 수 있는 고정밀 전압센서를 제안한다. 제안된 고정밀 전압센서는 동기화된 스위칭에 의해서 얼마나 큰 폭으로 동작 전압이 강하할 수 있는지 실시간으로 검출할 수 있으며, 클록 사이클 시간 결정 시에 신뢰성을 위해 삽입되는 타이밍 마진을 어느 정도로 설정해야할지 결정할 때 사용될 수 있다. 본 논문에서 제안하는 동작 전압센서는 FPGA 상에서 표준 LUT(Look-Up Table) 자원과 전용의 고속 캐리전파 연결망을 이용하여 설계되었으며, Xilinx Spartan-6 개발 보드(XC6SLX9 칩 사용)를 사용하는 경우 3.3mV의 해상도를 갖는 동작 전압센서를 구현할 수 있었다.

Keywords
supply voltage sensor, high precision, FPGA, performance evaluation

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I. Introduction

Modern semiconductor CMOS technologies advance over decades and current integrated circuits (ICs) have higher integration densities thanks to the nano-scaled technology. In this CMOS technology, switching currents consumed by the simultaneous switching activities which are synchronized by a global clock have been increased continuously. In addition, the supply voltages for the logic cores inside the ICs have been scaled down to meet low power requirements. As a result, the timing margins of digital circuit designs using those ICs become narrower and smaller. In consequence, the supply voltage variations in the ICs are more critical to the their correct functionality than ever before.

Recently, some FPGA (Field Programmable Gate Array) architectures allow circuit designers to define valid temperatures, and voltage values in the constraints to guide the tool generate the timing models. Nevertheless, not all architectures support this option. Instead, in general, they use a default value which is valid in a typical working condition within the range of 5% of the supply voltage variation to generate parasitic parameters of circuits such as cell delays and interconnection delays for the timing analysis of the best and worst cases [1]. Thus, we can know how much the performance of the target circuits is degraded only within this range of the variations.

In order to make our target circuit become more reliable, we need to put more timing margins for the safety of the circuit operations in the modern semiconductor nanometer technologies where electro-magnetic interferences (EMI) and noises are more likely to affect the reliability of digital circuits [2][3]. However, how much the margin is enough to guarantee the functional correctness of ICs? To identify such a margin under supply voltage variations, a supply voltage sensor will be necessary to sniff the voltage variations when the circuits operate in the critical case. Based on the upper and lower bound of voltage variation, we can establish the margins for the circuits.

Typically, a conventional ring oscillator (RO) can be used to detect the supply voltage variations thanks to the relationship between the supply voltage and the cell delay [4]. However, the conventional RO only detects the average voltage variations during a long period of time. A real-time supply voltage variation sensor using a gated RO was proposed in [5]. Nevertheless, their circuits are more suitable for ASIC based designs than an FPGA based designs since their full-custom cells were designed and utilized to obtain fine-grained delay resolutions.

Another type of a supply voltage sensor using a “delay line”, which is called “time digital converter” (TDC), was proposed in [6]. The voltage variations can be detected cycle-by-cycle with the voltage resolution of 29mV. An ASIC version of the sensor in [4] had a finer voltage resolution of 3.9mV [7].

Our supply voltage sensor is made up by using standard Look-up Table (LUT) cells, and dedicated high-speed carry cells. The experiments show that the voltage resolution of our supply voltage sensor is about 3.3mV on a Xilinx FPGA Spartan-6 (XC6SLX9).

II. Preliminaries

2.1 A Structure of an FPGA

A FPGA is a reconfigurable hardware circuit who’s functionality can be reprogrammed many time. Its performance is better than that of a software but less than ASIC-style implementation of the function. Typically it has been used mainly as a prototyping platform but it is now used as a core part of a System-on-Chip (SoC) for better performance and energy efficiency than pure hardware or software only implementations.

2.2 High-Speed Carry Logic in an FPGA

Since an FPGA is a reprogrammable platform, it can not been optimized more than ASIC-style circuit implementation. To overcome such a performance issue, modern commercial FPGAs adopt dedicated well-optimized circuit and functional modules such as a digital signal processing (DSP) logic, a block memory and a high-speed carry logic (CARRY4 in an Xilinx FPGA). Through the uses of such dedicated high-speed IP modules, high-performance circuits can be implemented on an FPGA.

III. Proposal of a Supply Voltage Sensor

For commercial FPGAs such as Xilinx Spartan-6s or other high-end FPGA families, as we mentioned in Section II, they have dedicated CARRY4 chains with very small carry propagation delays in order to support high speed arithmetic logics. The CARRY4 cell is actually a 4-bit carry generation circuit which is implemented with a dedicated carry propagation wire path. The measured propagation delay of one CARRY4 cell is about “134ps”. Note that this delay includes the delays of short wires that are used for configuring CARRY4 cells when measuring the delay. On average, each carry cell inside a CARRY4 cell has a propagation delay of “33.5ps” (= 134ps / 4) since each CARRY4 has four cascaded carry cells.

We can take advantage of the high-speed carry propagating logics to construct a delay chain or a delay line for obtaining fine-grained delay elements.

However, if we only use the dedicated CARRY4 chain, then the length of the delay chain will be prolonged and the corresponding chip area will be large accordingly. Besides, instead of increasing the clock period to increase the accumulated delay changing, we can use larger delay cells such as LUTs as coarse-grain delay elements in order to sense the voltage variations.

Therefore, we propose a delay chain with two parts with two different delay granularity: the first part consists of delay elements implemented by LUT primitives on an FPGA for controlling coarse-grained delay step, and the second part consists of delay elements based on the dedicated fast CARRY4 cells for controlling fine-grained delay step. The detailed structure of such a delay chain is illustrated in Fig. 1.

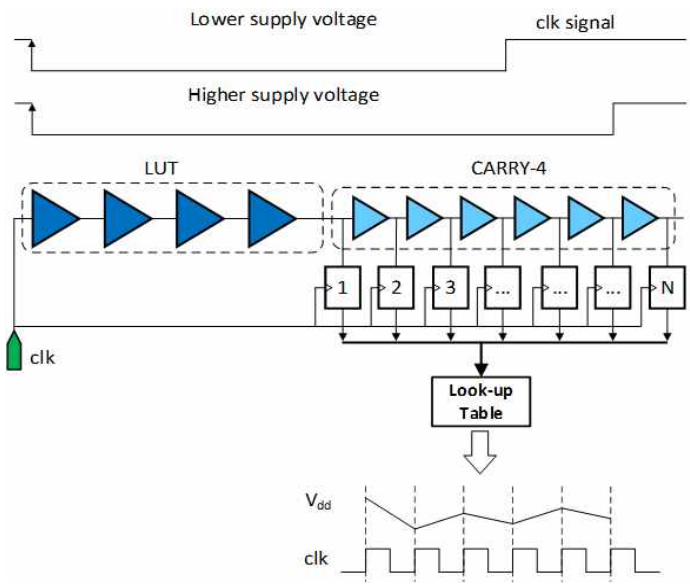

Fig. 1. Schematic of a supply voltage sensor

As shown in Fig. 1, the initial part of the delay chain is composed of LUT primitives and the second part of the chain consists of CARRY4 cells.

In our sensor, a stable clock signal event, which is generated by a Phase Locked Loop (PLL), is propagated over the delay chain, and also used to clock for FFs to capture the values of delay elements' outputs. At the nominal supply voltage level, the total propagation delay of the sensor is nearly fitted in a half of clock cycle. The falling edge signal of a clock is propagated over the delay chain and stable values at each delay cell are captured into FFs when the clock rises.

Depending on the signal propagation speed over the delay chain which is proportionally affected by the operating supply voltage, the captured values at the FFs show a specific "**000...000111...1**" pattern. Most of the initial FFs near at the input side capture bit-0s while later FFs located at the end of the sensor capture bit-1s as shown in Fig. 1. From the pattern, the speed of the signal propagation can be detected by checking where is the "0 to 1" transition in the pattern. Earlier "0 to 1" transition in the pattern means slower propagation speed while later "0 and 1" transition means faster propagation speed. Finally, the corresponding operating supply voltage at the speed is derived by looking up a pre-made the pattern to supply voltage mapping table. The calibration table content is given in Table. 1.

IV. Performance Evaluation

4.1 Validity of our supply voltage sensor

In order to validate the operation and evaluate the voltage resolution of our supply voltage sensor, we change the operating supply voltage of the FPGA logic core (VCCINT) intentionally. For convenience, we connect VCCINT pin of the internal core with a programmable DC power supply, and change the voltage from 1.04 V to 1.22 V with the step of 10 mV. Fig. 2 shows our experimental setup for measurements

Our sensor has been implemented with 54 FFs which inputs are fed by the outputs of the delay elements in the delay chain as shown in Fig. 1.

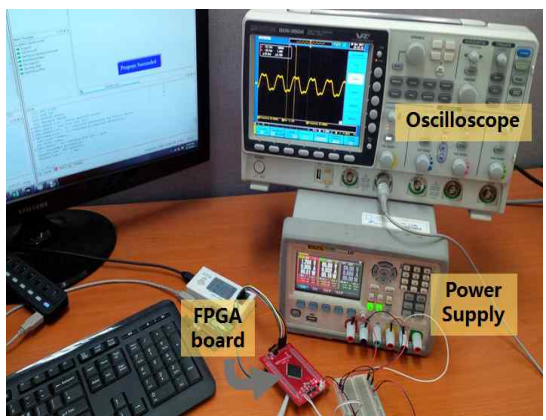

Fig. 2. Experimental setup for measurements

Table 1. Calibration table

Supply Voltage (V)	54-bit Calibration Code	Supply Voltage (V)	54-bit Calibration Code
1.22	0x00000000000001	1.12	0x0000003FFFFFFF
1.21	0x0000000000000F	1.11	0x000003FFFFFFFF
1.20	0x0000000000003F	1.10	0x00000FFFFFFFFF
1.19	0x000000000003FF	1.09	0x0000FFFFFFFFFF
1.18	0x00000000000FFF	1.08	0x000FFFFFFFFFFF
1.17	0x0000000000FFFF	1.07	0x003FFFFFFFFFFF
1.16	0x0000000003FFFF	1.06	0x01FFFFFFFFFFFF
1.15	0x000000000FFFFF	1.05	0x07FFFFFFFFFFFF
1.14	0x00000000FFFFFF	1.04	0x1FFFFFFFFFFFFF
1.13	0x00000003FFFFFF	-	-

By increasing or decreasing the supply voltage, the number of bit-0s that are stored in the FFs of the delay chain is increased/decreased. When increasing the supply voltage, the propagation delay of the delay chain is decreased and the falling edge of the clock goes faster over the chain. As a result, there are more number of bit-0s that pass through the delay chain. If decreasing the supply voltage, the propagation delay is increased. So the falling edge of the clock signal propagates slowly and consequently the number of bit-0s passing through the delay chain is decreased.

The measurement results are shown in Fig. 3. The actual measurement results are represented by green circles. We find that the number of bit-0s passing through the delay chain is linearly proportional to the operating supply voltage. From the measurement data, the fitted curve is derived and represented by the red line with the slope of **0.0033V** (~3.3mV).

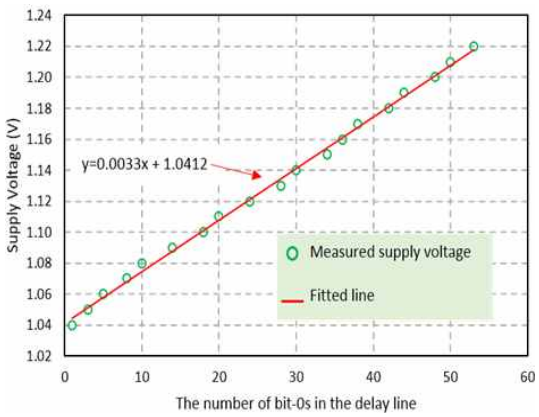

Fig. 3. Measured supply voltage represented by the number of bit-0s passing the delay line

Table 2. Comparison of voltage resolutions

Refs	FPGA/ASIC	Tech.	Resolution (mV)
[6]	Altera Stratix III	65nm	29
[7]	ASIC	65nm	3.9
[9]	ASIC	45nm	7.6
[10]	ASIC	90nm	10.0
[11]	ASIC	90nm	20.0
Ours	Xilinx Spartan-6	45nm	3.3

Table 2 shows the voltage resolution comparison between ours and previous works. As can be seen in the table, the voltage resolution of our works is better than those of [6][7][9]-[11]. Note that the work [7], [9]-[11] use ASIC style of circuit implementation.

4.2 Design Example

The block diagram of a target design example is shown in Fig. 4. Dummy logics are power-hungry circuits that consume large amounts of the simultaneous dynamic supply currents. Therefore, there are voltage drops across the PDN of the target circuit, and the actual operating voltages supplied to the cells inside the chip are not equal to the nominal level.

The circuit structure of a power-hungry circuit is described in [8]. A controller can activate or deactivate the individual dummy logic blocks independently, and it controls the target design to write the measured results into a memory. Then, an on-chip UART transmitter transfers the stored measured results to an external PC.

The measurement results are shown in Fig. 5. There is no voltage drop observed at the initial part of the execution since no logic block is activated. In the second part marked by “DL-1”, one dummy logic block called DL-1 start to operate, and then voltage drop happens. In this part, the observed voltage drop is measured around 20-30mV. Similarly, the supply voltage drops about 50mV, and 70-80mV when two and three logic blocks are activated in turn.

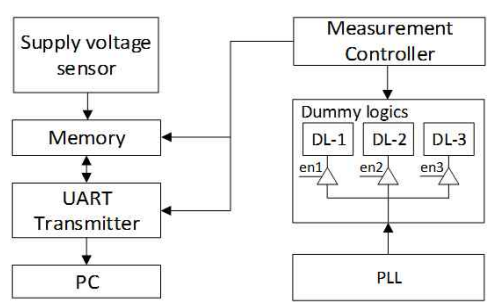

Fig. 4. Design for evaluation of the supply voltage drops

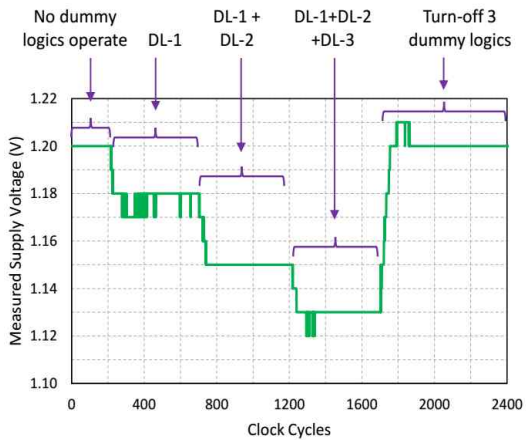

Fig. 5. Voltage drop measurement results

These dummy logic blocks have the same size of the circuit which is actually composed of 1000 FFs for each block. The only differences between them are the data and clock routing, therefore, their current consumption might be slightly different from each other. Note that the operating frequency of dummy logics is 60MHz.

V. Conclusion

This paper presents the design of a high-resolution supply voltage sensor that can be synthesizable on an commercial FPGA. We have verified its functionality, and used it to detect a given voltage drop profile of our target design. All the implementations have been carried out on the Xilinx Spartan-6 (XC6SLX9). The obtained voltage resolution is about 3.3mV thanks to the fine-grain delay resolution we have with dedicated high-speed CARRY4 cells in the FPGA. Compared to the previous work in [6][7], [9]-[11], our voltage sensor has a better sensing resolution.

The proposed method can be effectively employed and used in the highly reliable digital circuits that are used in a safety-critical system working in a harsh and noise environment such as a cruise-control system of an airplane and an airbag control systems in a car.

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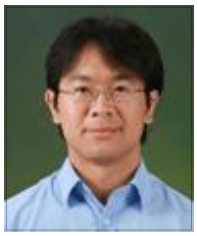

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